AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An integrated circuit for liquid crystal display comprising:

internal clock generating circuitry for generating a plurality of internal clock signals each sequentially delayed and an output clock signal in accordance with an input clock signal; and

data latch circuitry for receiving a plurality of display data signals corresponding to a display data input signal each having a respective point of change, said data latch circuitry for outputting the plurality of display data signals each sequentially delayed in accordance with the plurality of internal clock signals, wherein points of changing the plurality of display data signals with respect to a time base are set with time delays that lag one another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced.

2. (Previously Presented) An integrated circuit for liquid crystal display characterized in that multi-port data output signals are generated with respect to a data input signal, and points of changing said data output signals with respect to a time base are set with time delays that lag one another during one period of a reference internal clock signal, so that number of simultaneous changes of display data output signals is reduced, wherein the points of changing the data output signals with respect to the time base are set to points respectively delayed from an active edge of the clock output signal by 0.5 period, 1 period, and 1.5 period of the data input signal.

3. (Previously Presented) The integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the plurality of display data signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the output clock signal by optional integer times as long as a half period of the data input signal.

4. (Previously Presented) The integrated circuit for liquid crystal display according to claim 1, wherein the points of changing the plurality of display data signals with respect to the time base are set to points respectively having time delays that lag one another from the active edge of the output clock signal by optional integer times as long as a half period of the display data input signal and by a delay time produced by a delay circuit added to the optional integer times as long as a half period of the display data input signal.

Claim 5 (Cancelled)

6. (Previously Presented) A liquid crystal display characterized in that multi-port display data output signals are generated with respect to a data input signal, and points of changing said display data output signals with respect to a time base are set with time delays that lag one another during one period of a clock output signal or a reference internal clock signal having a same phase as the clock output signal, so that number of simultaneous changes of display data output signals is reduced, wherein the points of changing the display data output signals with respect to the time base are set to points respectively delayed from the active edge of

the clock output signal by 0.5 period, 1 period, and 1.5 period of the clock input signal or the display data input signal.

Claims 7-18 (Cancelled)